Dedicated flexible electronics for adaptive secondary control

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ABSTRACT

In the frame of the Large Binocular Telescope (LBT) adaptive secondary project, we developed a new dedicated electronics that controls the thin shell by means of 672 force actuators and capacitive sensor, while performing also the Real Time Reconstructor (RTR) computations. Within the adaptive optics system, the Slope Computer is also implemented using the same electronics, directly interfaced to the wavefront sensor CCD output by means of built-in fast parallel I/O channels. The system design has been tailored to balance the computational power, in the range of hundreds of Gigaflops, with an effective and time-deterministic real-time communication scheme. Diagnostic and maintenance are performed through an additional, fully independent communication line. Modularity, flexibility and remote in-system reconfigurability make this compact electronic suitable for real time adaptive optics control systems within a wide range of size and complexity, up to several thousands of actuators.

In this paper we describe the general hardware and software architecture and the application results of this electronics within the LBT first light adaptive optics system.

Keywords: Adaptive optics, real time control system, parallel computing, deformable mirrors, adaptive secondary

1 INTRODUCTION

The architecture of the LBT adaptive secondary control electronics derives from the MMT adaptive secondary control system. Nevertheless, the electronics has been completely redesigned with the aim of conceiving a powerful and flexible electronics, capable of controlling high order adaptive optics correctors (the system can be expanded up to several thousand of actuators). The new control electronics consists of a high performance, floating point parallel computer with a dedicated analog interface that allows direct interfacing to the actuators (Voice Coil Motors) and capacitive sensors that sense the local gaps between reference body and thin shell. A particular design effort has been dedicated to the communication system, so that the considerable computational power, in the range of hundreds of Gigaflops, is well supported by a dedicated real-time communication that allows to exchange data efficiently among the parallel processors. Within the LBT672 adaptive secondary, the described electronics does not only control the actuators but performs also the Real time Reconstructor (RTR) task.

The control electronics is based on two main components, the DSP control board and the Basic Computational Unit (BCU). The DSP control board performs all parallel processing tasks (actuators control and Real Time Reconstructor) and embeds the analog electronics that drives the actuators and samples the capacitive sensors signals (eight channels controlled by each board). The BCU can be considered as a general purpose board: in the adaptive secondary control it acts as communication board, distributing both real time and diagnostic data among the DSP boards; the BCU can also operate in standalone mode, in particular in the LBT system it is configured to operate as slope computer.

The adaptive secondary control electronics has been developed by Microgate (Italy) in strict co-operation with the other partners involved in the project, namely Osservatorio Astrofisico di Arcetri (Italy), ADS International (Italy), Aerospace Engineering Department of Politecnico di Milano (Italy) and Mirror Lab (Steward Observatory, AZ, USA).

The system design and lab testing has been already completed. The new electronics has been integrated on P45, the 45 actuators engineering prototype of LBT672. All functional and performance test on P45 will be completed before July
The electronics production run for the first LBT672 adaptive secondary unit has already started, and we plan to integrate the first adaptive secondary unit electronics in October 2004. The BCU-based slope computers is running at Osservatorio di Arcetri since July 2003. The integration of the telescope units shall be completed before August 2004.

2 SYSTEM AND PERFORMANCE REQUIREMENTS AND DESIGN CONSTRAINTS

Even if the presented adaptive secondary control electronics can be easily adapted to different configurations, the design requirements derive directly from the LBT672 ones. The relevant requirements for computational power dimensioning are reported hereafter:

- number of actuators, per unit = 672
- computational power (Slope Computer) = the time latency between last pixel acquired from the CCD controller and new slopes set available (ready to be transferred, but excluding transfer time) shall be less than 25µs
- computational power (applies to Real Time Reconstructor and adaptive mirror control) = updated position command and related feedforward force shall be applied within 75µs after the last slope has been transmitted. This applies for both zonal and modal control, considering a 'leaking' integrator (1 pole, 1 zero) and 450 modes
- communication bandwidth =1414 slopes shall be transferred to the mirror in less than 50µs

For what concerns the analog performances of the system, the relevant specifications can be derived from the following system requirements:

- settling time (single actuator and modal, for each controllable mode) < 1.5ms, 0.1N max delta-force
- actuator position sensor noise < 10nm RMS
- actuator position sensor long term stability < 20nm RMS over 8 hours, corresponding to < 5nm/°K
- actuator static force = ± 0.6 N
- power consumption (applies to the adaptive secondary unit, AC-DC power supply dissipation not included) < 3.5KW

3 LBT ADAPTIVE OPTICS ELECTRONICS ARCHITECTURE

A simplified scheme of the first light LBT adaptive optics control system is presented in Figure 1.
The CCD controller of the pyramid wavefront sensor (XXX rif. A Simone) is directly connected to the Slope Computer. This is based on a single BCU board. A second BCU board is used as frame grabber, to read the output of a technical CCD used for pointing purposes. Both BCUs are connected to the Adaptive Optics Supervisor (XXX verificare) by means of a Gigabit Ethernet diagnostic link. Real time data (slopes output) are passed from the slope computer to the adaptive secondary control system by means of a 4.25 Gigabit/s fiber link.

A block diagram of the LBT672 adaptive secondary electronics is presented in Figure 2.

![Figure 2 – LBT672 adaptive secondary electronics block diagram](image)

The adaptive secondary is controlled by 672 voice coil actuators. The actuators embed also a capacitive sensor board performing the first signal conditioning for the co-located capacitive sensor signal that measures the distance between thin shell and reference body (XXX riferimento a Daniele).

The actuators are connected to signal distribution boards, placed immediately behind the coldplate. The signal distribution boards provide the connection to the DSP control boards. Each controls 8 channels by means of 2 floating point DSPs. Moreover, the Real Time Reconstructor is also implemented on these boards. Every backplane (there are 6 backplanes in the system, arranged into 3 liquid cooled crates) contains 14 DSP control boards, one signal generation board providing a stable reference signal for the capacitive sensors, and a BCU-based communication board that implements the high speed, real time communication between slope computer and adaptive mirror. Moreover, the communication board provides a diagnostic communication line over a standard Ethernet connection.

All boards in the crates have identical size (191x96 mm). Due to the high complexity and large number of components mounted on them, the boards implement the most recent Surface Mounting Technology (SMT), with a large number of components in Ball Grid Array (BGA) package.

4 MAIN SYSTEM COMPONENTS

4.1 BASIC COMPUTATIONAL UNIT

The Basic Computational Unit has been designed with the aim of covering a wide range of applications within the adaptive optics control system:
• Communication board within the LBT672 adaptive secondary control electronics. The communication board handles both real-time and diagnostic communication, distributing data from the external fiber-optic interfaces to the DSP boards through the system backplanes.

• Slope computer, connected to the CCD controller (SciMeasure LittleJoe) by means of its standard AIA interface.

• Simple frame grabber for technical CCDs. Also for this application the BCU is connected directly to the CCD controller.

• For Multi Conjugate Adaptive Optics, the BCU will merge data sampled by several CCDs performing intermediate processing and feeding data into a single real-time communication output for the Real Time Reconstructor.

From all these different applications, we can derive some common requirements for the BCU board:

• On-board computational power in the range of hundreds of Mflops.

• Capability of handling in hardware real-time communication and data pre-processing.

• Availability of several fiber-optic real-time communication ports, typically two independent data inputs to be merged into a single, doubled bandwidth data output.

• Possibility to connect directly sensor electronics (typically CCD controllers).

• Presence of diagnostic interface.

Figure 3 – Basic Computational Unit block diagram

The block diagram of the BCU is presented in Figure 3.
Referring to the external interfaces, the real-time communication interface is provided by 4 communication modules based on 2.125 Gigabit/s Fiber channel interfaces. The diagnostic communication interface is based on the Gigabit Ethernet standard. As physical interface, both copper and fiber optic are available. All communication interfaces are implemented on small modules (XXX figure della BCU e dei moduli , eventualmente il rear side con le frecce che indicano i moduli) mounted on the rear of the BCU board. 72 flexible input-output ports provide the interface to external devices, in particular to CCD controllers. The ports can be configured as input, output, single ended or differential (LVDS). A serial interface, user-configurable as RS232 or RS485, is provided for controlling instruments or other applications. An additional 10 Mbit/s fiber interface is available for global system synchronization.

The BCU is internally interfaced to the backplane by means of a proprietary bus interface. There are two completely independent busses: the first is 32 bit wide and is dedicated to real-time communication (3.9 Gigabit/s throughput); the second is 16 bit wide and routes the diagnostic communication (1.95 Gigabit/s throughput). Both are synchronous (operating at 60.7 MHz, DDR) and physically based on B-LVDS technology.

The BCU internal architecture is largely based on a large FPGA (Altera Stratix). This component connects all internal and external interfaces, the DSP and all on-board peripherals. The real-time communication is completely handled at hardware level, for maximum efficiency. Data are transferred bi-directionally from the Fiber Channel interfaces to the local DSP (through the 64 bit DSP bus and using DMA access), and to the DSP boards on the same backplane.

A 32 bit RISC processor is embedded in the same FPGA (Nios soft-core). This processor handles the Ethernet communication and performs also ‘housekeeping’ functions, like boards temperature acquisition.

The FPGA can be easily reconfigured to provide dedicated interfaces to external devices and to perform data preprocessing. E.g., on the Slope Computer we implemented on the FPGA an AIA compliant protocol for direct interfacing of the CCD controller through the PIO versatile I/O port. Acquired pixel readings are reorganized by the FPGA according to a look-up-table and transferred via DMA in the proper order to the DSP internal memory for slopes computation.

The computational power is provided by a single TigerShark floating point DSP by Analog Devices (ADDSP-TS101), delivering 475 floating point MMAC/s (millions of multiply and accumulate, 32x32 \( \Rightarrow \) 40 bit floating point).

A large (1 Gbit SDRAM) memory is provided for diagnostic data storage.

### 4.2 DSP CONTROL BOARD

Each DSP control board controls eight actuators on the adaptive secondary mirror. The board comprehends a high speed digital part (DSP, diagnostic processor and communication electronics) and an analog front-end that interfaces the board to the actuators and capacitive sensors. A block diagram of the board is given in Figure 4.
The digital and computational architecture resembles the BCU one. Two identical DSPs double the computational power (950 MMAC/s). As in the BCU, the main system logic (FPGA) handles the communication between backplane, DSPs and other peripherals. The same logic provides direct connection between DSPs and 16 bit Analog to Digital and Digital to Analog converters that control 8 actuators handled by each DSP board. Data transfer is completely handled by the FPGA without software overhead.

The analog part of the board comprehends the current drivers for the voice coil motors. The current drivers are based on a linear design. This has been preferred to a switching architecture on base of bandwidth and noise considerations, thus sacrificing the efficiency of the drivers. Large bandwidth (see XXX) is obtained thanks to a current feedback topology. A dedicated circuitry has been implemented to minimize the effect digital noise feedthrough and glitches.

The capacitive sensors output signals are converted from differential to single ended by an input amplifiers that also implements the anti-aliasing filtering.

On-board diagnostic comprehends the measurement of local temperatures (FPGA, DSPs and current drivers) and an independent measurement of the voice coil current. This allows to diagnose fault conditions on the coils, like shortcuts or open circuits.

5 SYSTEM COMMUNICATION

Data transfer among several computational units is very often a critical aspect of parallel computers. A particular design effort has been dedicated to guarantee very limited communication latencies and to provide suitable communication primitives.
The first remarkable aspect is the complete separation between real-time communication and diagnostic communication. The data paths are always separated, in the external interface, in the backplanes and also in the DMA channels used to transfer the data from the on-board devices to the backplane.

The real time communication is dedicated only to exchange data related to the adaptive optics control loop: it transfers the slopes from the slope computer to the adaptive secondary control system and allows to share intermediate computational results among all processors, as required by reconstructor algorithms implementing IIR filters. The real time communication interface is based on Fiber Channel physical layer. There are two bi-directional fiber links acting as ‘logic inputs’ (i.e., they are ‘slaves’ with respect to the preceding unit in the communication path) and two identical fiber links acting as ‘logic output’ on every communication board. The raw data speed on each channel is of 2.125 Gbit/s, for an aggregate bandwidth of 4.5 Gbit/s. Considering the bandwidth reduction due to encoding/decoding, packet handling and error checking, the typical actual data throughput is of 3.2 Gbit/s. Data transfer and packet handling is completely performed by hardware (FPGA), thus ensuring a strict time determinism. These allows to use the real-time communication to synchronize the operation of the Real Time Reconstructor with respect to the Slope Computer, without requiring an additional synchronization line.

The communication protocol is based on four simple primitives:

- **Write_same**: transmits data from the master (typically the slope computer) to one/several DSPs, writing the same data to the same internal addresses of all addressed DSPs
- **Write_sequential**: transmits data from the host to one/several DSPs, writing different data to the same internal addresses of all addressed DSPs
- **Read_sequential**: receives data from one/several DSPs, reading data from the same internal address of the addressed DSPs
- **Read_write_simultaneous**: allows reception of data from one/several DSPs, reading data from sequential internal addressed of the addressed DSPs. At same time, the data are written to the same addresses on all other DSPs

The diagnostic communication is used to transfer all diagnostic data (circular buffers, boards status) and for system maintenance, as explained in Sect. 6. The external interface is based on Gigabit Ethernet standard. Both fiber and copper media are available through different communication modules to be installed on the BCU board. The communication protocol is based on a dedicated UDP/IP layer (MGP_UDP=Microgate Protocol UDP), the transactions are handled by the FPGA embedded processor (Nios soft-core). Similarly to the real-time communication, a small set of primitives allows to read/write data sequentially from/to the available devices (bulk memory on SDRAM, SRAM, FPGA memory locations for configuration purposes, DSP internal memory, configuration FLASH), both on BCU and DSP boards.

An IP address is assigned to each BCU board, and the other devices on the crate can be addressed by setting the appropriate address in the header of the MGP_UPD packet.

### 6 SYSTEM CONFIGURATION AND MAINTAINANCE

The diagnostic communication allows also to reconfigure completely the boards remotely. Not only the DSP and housekeeping processor software, but also the system FPGA configuration can be uploaded through diagnostic communication. A safety mechanism is provided in order to guarantee that the system can be always recovered from any wrong configuration, by forcing the boot-loading of a ‘safe’ factory setup. Also the IP address of the BCU boards can be modified remotely by means of a dedicated Ethernet command that targets directly the MAC address of the board.

For the sake of reliability and easy maintenance, there are no electromechanical devices like potentiometers or dipswitches on the system. The calibration of the analog parts is performed automatically during system factory testing and is handled directly by the DSPs. The calibration and setup parameters are stored on permanent memory on each DSP control board.
Similarly, the DSP boards address on the crate is related to their position on the crate. Consequently, boards can be easily replaced without needing any configuration.

7 SOFTWARE

With respect to the embedded software running on the different component of the adaptive optics control system, we can distinguish the following layers:

- slope computer real time software
- adaptive secondary control software, including local actuators control and global computations, like real time Reconstructor and feedforward algorithm
- diagnostic software
- housekeeping software

The real-time software is currently implemented within a simple, interrupt driven structure, so it is not based on a real-time operating system. For the current needs this architecture is still the most efficient and simple one, but this does not prevent from using an operating system for future more structured applications.

7.1 SLOPE COMPUTER REAL TIME SOFTWARE

The slope computer software allows to compute in real time the slopes from the pixels acquired by the wavefront sensor CCD controller. Referring to Figure 5, the slope computer BCU is directly interfaced to the CCD controller (SciMeasure LittleJoe in the LBT case) through a standard AIA interface. The BCU operation is synchronized by the ‘frame-sync’ signal generated by the CCD controller.

The first data pre-processing is performed at hardware level by the main BCU FPGA. Acquired pixel are re-organized according to an user-defined look-up-table and stored into DSP’s internal memory by means of a DMA process. The look-up-table contains the DSP memory location addresses where the pixel shall be stored so that the slope computation is executed sequentially in the most efficient way. Moreover, the look-up-table contains also the information of how many slopes can be computed with the pixels already transferred to the DSP. In this way, the slope computer can be easily adapted to different slope wavefront sensor configurations (pyramid, Shack-Hartmann) by simply modifying the look-up-table. Moreover, the slope computation is pipelined and therefore no latency is guaranteed up to a certain number of slopes (see Table 5).

The implemented algorithm performs the following operations:

- Single pixel gain and offset compensation, according to an user-definable table
- Slopes computation
- Slopes gain compensation, according to an user-definable look-up-table
- Mean tilt computation
- Average flux computation

Once the slopes become available, these are sent to the Real Time Reconstructor through the real time communication link. The slopes transmission acts also as system synchronization for the Real Time Reconstructor.
7.2 ADAPTIVE SECONDARY CONTROL SOFTWARE

Within the adaptive secondary control software, we can distinguish two main functional blocks, namely the high speed local control loop, that implements a local position controller, and the global computations required to implement the Real Time Reconstructor and the feed-forward algorithm (see XXX articolo Armando).

\[
\begin{align*}
\{d\phi\}_i &= [B]\{S\}_i - [A]\{d\phi\}_{i-1} \\
\{d\beta\}_i &= [K]\{d\phi\}_i
\end{align*}
\]

Figure 5 – Slope computer software block diagram

Figure 6– LBT adaptive secondary control software scheme
In the local control loop, the gap information acquired from the capacitive sensor is first linearized, then fed into the digital filter that implements the local controller. The local loop compensator law is typically implemented as a proportional/derivative controller. The derivative part provides the “artificial” damping required to stabilize the large number of uncontrollable modes typical of an highly coupled structure like the thin mirror shell. The specified dynamic performance requires to extend the bandwidth of the derivative part to 10KHz or more. Consequently, the local control loop runs at ~100KHz.

Differently, global computations are performed each time a set of slopes becomes available from the slope computer (typically at 1KHz rate). The feedforward computation takes the form

\[ \{\Delta f\}_{i} = [K]\{\Delta p\}_{i} \]

where \(p\) and \(f\) are, respectively, the actuator positions and forces and \([K]\) is the mirror stiffness matrix, while the reconstructor algorithm can vary depending on the type of reconstructor adopted (zonal vs. modal). E.g., for a zonal reconstructor with a dynamic filter with one pole not in zero (pseudo-integrator), we have:

\[ \{\Delta p\}_{i} = [B]\{S\}_{i} - [A]\{\Delta p\}_{i-1} \]

with \(\{S\}\) slope vector and \([B]\) and \([A]\) the input and output gains, respectively.

All these computations can be very effectively implemented in the parallel architecture of the adaptive secondary control system. In fact, every DSP can perform only the operations related to the four controlled channels, involving just four rows of the gain matrices.
To improve the computational efficiency, only those operations that require the last slopes vector are performed after the slopes are transmitted. All other operations are pre-computed in advance, after transferring the delta-positions and delta-forces to the local controller.

7.3 DIAGNOSTIC SOFTWARE

The diagnostic software allows the acquisition of circular and linear buffers and the automatic generation of time sequences according to stored data. It is a very useful tool both during ordinary system operation and during system debugging and calibration.

The diagnostic software is based on a simple but powerful and flexible structure: 16 buffers can be filled autonomously with the content of any memory address or contiguous sequence of memory locations. The user can instantiate the buffer by specifying the following parameters:

- Buffer length
- Buffer mode (linear or circular)
- Direction (read, i.e. the buffer is filled with the content of the specified memory address; write, i.e. the specified memory location is filled with sequentially with the buffer content)
- Target memory address
- Target memory length (i.e., the number of memory locations that shall be read/written at every step)
- Trigger source (can be either the fast local control loop at ~100KHz, or the external loop at ~1KHz)
- Decimation factor
- Trigger value, address, and logic operator (the acquisition start can be triggered by a logic condition occurring between a certain memory and a definable value)

It is crucial to notice that the diagnostic buffers management is implemented in hardware (FPGA), and memory transfer is based on DMA processes. So here is no software overhead in their operation, and the DSPs computational power remains fully available for computations.

It is possible to define up to eight data vectors. Each vector can be filled automatically with the values contained in an user-definable memory location at each control step. Alternatively, the memory location can be filled with the values read from the data vector. This feature provides a powerful tool for signal generation during system response tests. The user can define the buffer length, select them as linear or circular, and set decimation factors, if required. This architecture moves to the Adaptive Optics Supervisor software (see S.Esposito in 8) the actual definition of the diagnostic parameters, and permits to avoid frequent updates of the DSP real time code.

8 ADAPTIVE SECONDARY CONTROL ELECTRONICS IN NUMBERS

The main characteristics of the LBT adaptive secondary electronics are resumed on Table 1.

<table>
<thead>
<tr>
<th>Number of channels (each mirror)</th>
<th>672</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of DSP boards</td>
<td>84</td>
</tr>
<tr>
<td>Channels controlled by each DSP board</td>
<td>8</td>
</tr>
<tr>
<td>Number of crates</td>
<td>6 (3 double crates)</td>
</tr>
<tr>
<td>DSP boards on each crate</td>
<td>14</td>
</tr>
<tr>
<td>Sustained computational power, each DSP board (32x32 ⇒ 40 bit floating point MAC)</td>
<td>950 MMAC/s</td>
</tr>
<tr>
<td>Total computational power, each unit</td>
<td>80 GMAC/s</td>
</tr>
<tr>
<td>Real time communication actual data throughput (transmitting a set of 1414 slopes)</td>
<td>3.2 Gbit/s</td>
</tr>
<tr>
<td>Diagnostic communication actual data throughput</td>
<td>80 Mbit/s, each crate</td>
</tr>
</tbody>
</table>

Table 1 - LBT adaptive secondary electronics main characteristics
Table 2 resumes the analog performances and power consumption of the LBT672 electronics. The power consumption refers to an average seeing condition of 0.65” @ $\lambda = 500$nm, mirror thickness=1.6mm, coil efficiency 0.5 N/$\sqrt{W}$ and mirror flattening force = 0.02 N/actuator. Data have been extrapolated from P45 engineering prototype experimental data (logic and quiescent power consumption) and from simulations (turbulence correction). The other data have been actually measured.

<table>
<thead>
<tr>
<th>Capacitive sensor bandwidth</th>
<th>-3dB @ 90 KHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitive sensor noise</td>
<td>1.8nm rms @ 50µm gap</td>
</tr>
<tr>
<td>Capacitive sensor stability</td>
<td>1.5mm/°C</td>
</tr>
<tr>
<td>Capacitive sensor resolution</td>
<td>1.5 nm</td>
</tr>
<tr>
<td>Current driver bandwidth</td>
<td>-3dB @ 300 KHz</td>
</tr>
<tr>
<td>Actuator force resolution</td>
<td>40 µN</td>
</tr>
<tr>
<td>Maximum actuator force</td>
<td>± 1.3 N</td>
</tr>
<tr>
<td>Logic power dissipation, each LBT672</td>
<td>490 W</td>
</tr>
<tr>
<td>Power dissipation in the crates</td>
<td>2160 W</td>
</tr>
<tr>
<td>Power dissipation in the actuators (coil + capacitive sensor)</td>
<td>152 W</td>
</tr>
<tr>
<td>Total power dissipation</td>
<td>2312 W</td>
</tr>
</tbody>
</table>

Table 2 - Adaptive secondary electronics analog performances and power consumption

On Table 3 we report the DSP board performances for what concerns the local control loop, not including the related global feedforward computation. The digital loop latency includes also ADC conversion time and DAC settling time, so it the actual time delay introduces by the digital control. Considering that the derivative part of the compensator shall be effective up to 10 KHz or more, the phase lag introduced by digital control amount to 23 deg, so the digital control system is adequate to the performance goal. It shall be noticed that the local control consumes just 18% of the available computational power, being the remaining power available for Real Time Reconstructor and FeedForward computation (in fact diagnostic handling is completely offloaded to the FPGA and to the additional ‘housekeeping’ processor).

| Local control loop computational delay (sensor linearization, position + velocity loops) | 1.5 µs typ. |
| Total digital loop latency (ADC sampling & conversion, data transfer, computation, DAC settling) | 6.4 µs typ. |
| Digital control loop frequency | ~ 100 KHz |
| DSP resources used by local control loop | 18% |

Table 3 – DSP control board local control loop performances

The computational and communication performance of the presented electronics is addressed on Table 4 and Table 5. Latency and transfer time refer to the LBT672 first light conditions, i.e. 672 actuators and 707x2 slopes. We considered a modal MIMO IIR filter, with 450 corrected modes and 4 zeros/4 poles. Data transfer time can be further improved by pipelining the operation, i.e. by sending the slopes as they become available instead of waiting for the computation to complete.

| Real Time Reconstructor + FeedForward computational latency | 34 µs |
| Slopes transfer time | 14 µs |
| Maximum number of actuators @ 200µs total latency (slopes transfer+RTR+FFWD) | ~ 2500 |

Table 4 – Adaptive secondary control system computational and communication performance, ‘global’ computations

Data reported on Table 5 refer to a single BCU slope computer. As described in 7.1, the slopes computation can be very efficiently pipelined, therefore the time latency from the last pixel acquired to last slope available is negligible (few microseconds). Consequently we present here the maximum number of pixels that could be handled by the present electronics without introducing a significant latency. The pyramid sensors is penalized by the fact that at least half of the pixels shall be acquired before starting computation (at least considering a ‘typical’ fur quadrants CCD architecture).
| Maximum number of slopes @ ‘~0 latency’, Schack Hartmann | 9000 x 2 |
| Maximum number of slopes @ ‘~0 latency’, Pyramid         | 4500 x 2 (128x128 CCD OK) |

Table 5 – Slope computer (single BCU-based) computational performances

9 CONCLUSIONS

The control electronics presented in this paper represents a suitable solution for current and next generation adaptive optics systems, up to some thousands of actuators. This does not only apply to the mere computational power, but also to a communication system which is specifically tailored for real time data exchange in a distributed, parallel environment. The final performance and system compactness could be obtained thanks to a dedicated design, and would have been probably not achievable with an off-the-shelf approach.

Flexibility, expandability and in-system re-configurability make the presented system suitable also for other applications. As an example, the MMT new Real Time Reconstructor based on same electronics (without analog interface) is currently under construction, and the same electronics represents also the baseline for the VLT adaptive secondary, which is now in the feasibility design phase.

Concerning the activity progress, the system design and prototyping can be considered successfully concluded, and the final tests on P45 (the 45 actuators engineering prototype of LBT672) are currently ongoing. Some design challenges, in particular the effectiveness of the ‘electronic damping’ provided by the wide analog bandwidth are still to be tested and confirmed. The series board production for LBT672 units #1 and #2 has already started, and the first unit is expected to be ‘on-sky’ in Spring 2005.

REFERENCES

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